GAL26CV12/883

High Performance E²CMOS PLD Generic Array Logic™

T-46-19-07

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - 20 ns Maximum Propagation Delay
  - Fmax = 33 MHz
  - 15 ns Maximum from Clock Input to Data Output
  - TTL Compatible 8 mA Outputs
  - UltraMOS® Advanced CMOS Technology
- **ACTIVE PULL-UPS ON ALL INPUTS AND I/Os**
- **LOW POWER CMOS**
  - 90 mA Typical Icc
- **E² CELL TECHNOLOGY**
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/Guaranteed 100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- **TWELVE OUTPUT LOGIC MACROCELLS**
  - Uses Standard 22V10 Macrocells
  - Maximum Flexibility for Complex Logic Designs
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
  - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

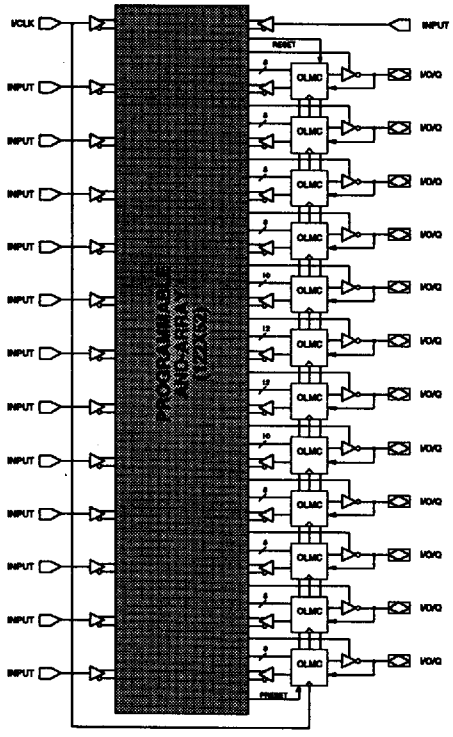
DESCRIPTION

The GAL26CV12/883 is a high performance E²CMOS programmable logic device processed in full compliance to MIL-STD-883. The GAL26CV12-20/883 combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the fastest 28-pin military PLD on the market. CMOS circuitry allows the GAL26CV12 to consume less power than comparable bipolar devices. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

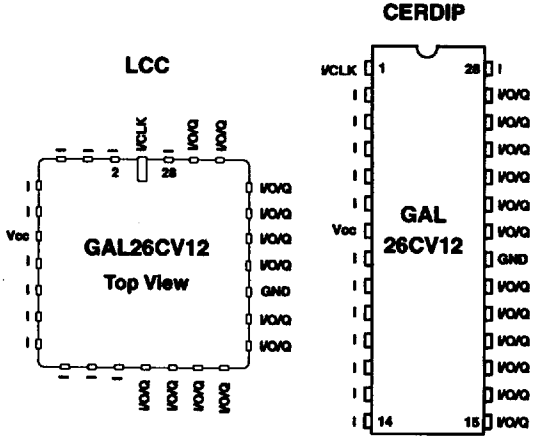
By building on the popular 22V10 architecture, the military version of the GAL26CV12 allows designers to be immediately productive, eliminating the learning curve. The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL26CV12 OLMC is fully compatible with the OLMC in standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products.

FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIAGRAMS



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May 1992

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Specifications GAL26CV12/883

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ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} .....–0.5 to +7V
Input voltage applied .....–2.5 to V_{CC} +1.0V
Off-state output voltage applied .....–2.5 to V_{CC} +1.0V
Storage Temperature .....–65 to 150°C
Case Temperature with
Power Applied .....–55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) .....–55 to +125°C
Supply voltage (V_{CC})
with Respect to Ground .....+4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	–2.0	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–50	—	–135	mA
ICC	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15Mhz Outputs Open	—	90	160	mA

1) The leakage current is due to the internal pull-up on all input and I/O pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25 C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
C_{VO}	I/O Capacitance	10	pF	V_{CC} = 5.0V, V_{VO} = 2.0V

*Guaranteed but not 100% tested.

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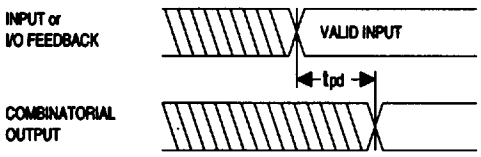
AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

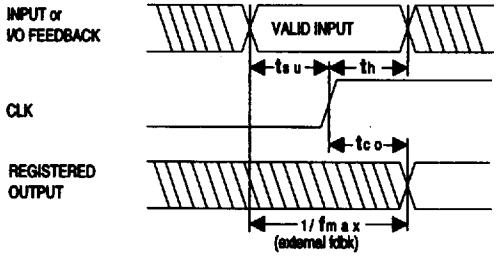
PARAMETER	TEST COND.[1]	DESCRIPTION	-20		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd	1	Input or I/O to Combinatorial Output	—	20	—	25	ns
tco	1	Clock to Output Delay	—	15	—	20	ns
tcf[2]	—	Clock to Feedback Delay	—	15	—	20	ns
tsu	—	Setup Time, Input or Feedback before Clock	17	—	20	—	ns
th	—	Hold Time, Input or Feedback after Clock	0	—	0	—	ns
fmax[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	31.2	—	25	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	31.2	—	25	—	MHz
	1	Maximum Clock Frequency with No Feedback	33.3	—	30	—	MHz
twh	—	Clock Pulse Duration, High	15	—	15	—	ns
twl	—	Clock Pulse Duration, Low	15	—	15	—	ns
ten	2	Input or I/O to Output Enabled	—	20	—	25	ns
tdis	3	Input or I/O to Output Disabled	—	20	—	25	ns
tar	1	Input or I/O to Asynchronous Reset of Register	—	25	—	30	ns
tarw	—	Asynchronous Reset Pulse Duration	20	—	25	—	ns
tarr	—	Asynchronous Reset to Clock Recovery Time	20	—	25	—	ns
tspr	—	Synchronous Preset to Clock Recovery Time	17	—	20	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

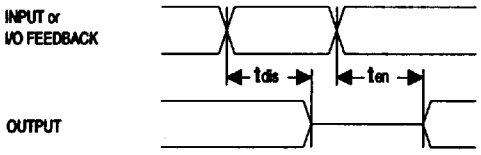
SWITCHING WAVEFORMS



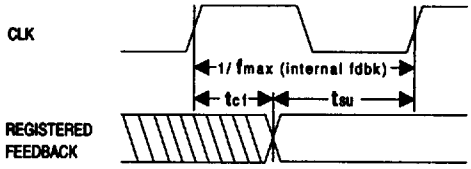
Combinatorial Output



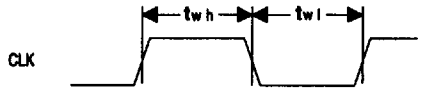
Registered Output



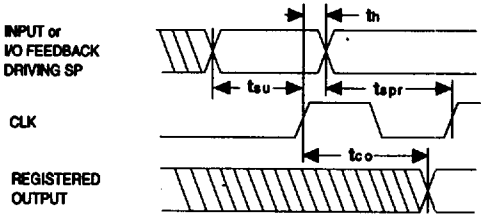
Input or I/O to Output Enable/Disable



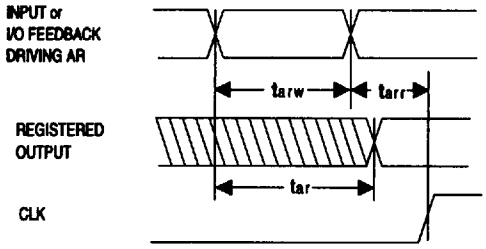
fmax with Feedback



Clock Width



Synchronous Preset



Asynchronous Reset

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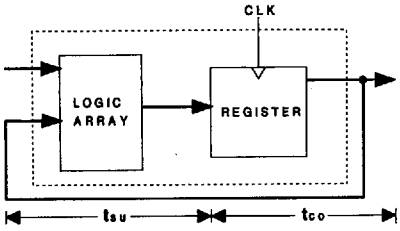
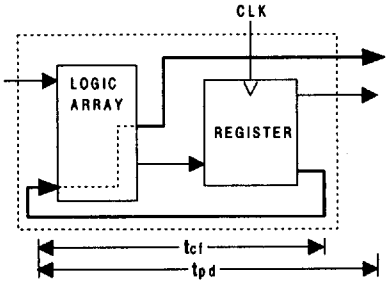
fmax SPECIFICATIONS



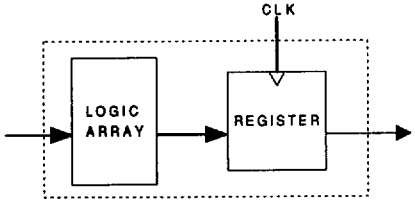
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.



fmax With No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.

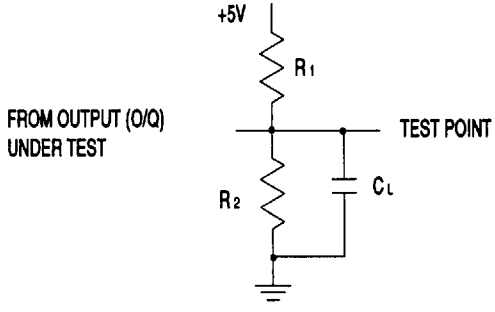
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
1		470Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	470Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	470Ω	390Ω	5pF



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

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GAL26CV12 ORDERING INFORMATION (MIL-STD-883 and SMD)

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Package	Ordering # MIL-STD-883	Ordering # SMD #
20	17	15	160	28-Pin CERDIP	GAL26CV12-20LD/883	Contact Factory
			160	28-Pin LCC	GAL26CV12-20LR/883	Contact Factory
25	20	20	160	28-Pin CERDIP	GAL26CV12-25LD/883	Contact Factory
			160	28-Pin LCC	GAL26CV12-25LR/883	Contact Factory

PART NUMBER DESCRIPTION